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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDREW MARK NIGHTINGALE

Appeal 2009-002102
Application 09/994,023
Technology Center 2100

Decided:[1] MAY 20, 2009

Before LEE E. BARRETT, JEAN R. HOMERE, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 2, 4-12, 14-22, and 24-30.[2] We have jurisdiction under 35 U.S.C. § 6(b), and we heard the appeal on May 12, 2009. We reverse.

STATEMENT OF THE CASE

Appellant invented a system for simulating data processing systems for verifying or testing system designs. In one implementation, a simulation system comprises multiple signal interface controllers 6, 8 and a test scenario manager 10 that coordinates the operations of the respective signal interface controllers. The signal interface controllers provide stimulus signals to a hardware simulation 4 representing a system-on-chip designed of a modeled integrated circuit (IC). The signal interface controllers report diagnostic information and other data to the test scenario manager. By virtue of a shared memory (i.e., a "scoreboard") in the test scenario manager, individual signal interface controllers can access data from other signal interface controllers and therefore share data.[3] Figure 1 of the present application shows a test scenario manager and multiple signal interface controllers connected to a hardware simulation and is reproduced below:

[2] Although Appellant indicates that claims 21 and 22 have been cancelled in the Status of Claims section (App. Br. 2) and the Examiner indicates that this status is correct (Ans. 2), Appellant nonetheless indicates that claims 21 and 22 are pending, rejected, and on appeal. *See* App. Br. 2 (including claims 21 and 22 in the listing of appealed claims). Claims 21 and 22 are, in fact, rejected and on appeal and are therefore before us.

[3] *See generally* Spec. 6:15–9:27; Figs. 1 and 5.

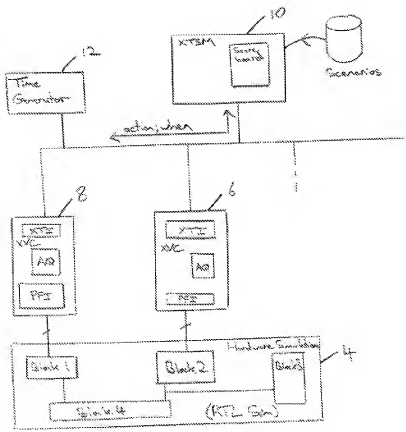


Figure 1 of the Present Application Showing a Test Scenario Manager 10 and Multiple Signal Interface Controllers 6, 8 Connected to Hardware Simulation 4.

Claim 1 is illustrative with the key disputed limitations emphasized:

1. Apparatus for simulating data processing operations performed by a data processing apparatus, said apparatus comprising:

a hardware simulator responsive to one or more stimulus signals to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus;

a plurality of signal interface controllers coupled to said hardware simulator, each signal interface controller serving to perform one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said

hardware simulator and said signal interface controller as part of simulating said data processing operations;

a test scenario manager coupled to said plurality of signal interface controllers and operable to transfer test scenario controlling messages to said plurality of signal interface controllers, at least one of said test scenario controlling messages including:

(i) data defining a simulation action to be performed by a signal interface controller; and

(ii) data defining when said signal interface controller should perform said simulated action; and

a time generator coupled to said plurality of signal interface controllers and said test scenario manager for generating messages specifying time defining events corresponding to advancement of simulated time for said hardware simulator,

wherein said *test scenario manager includes a shared data memory* into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager via said shared data memory *independently of advancement of simulated time* by said messages specifying time defining events, *said data being readable from said shared data memory by another signal interface controller*.

The Examiner relies on the following as evidence of unpatentability:

Rajsuman	US 6,678,645 B1	Jan. 13, 2004 (filed Oct. 28, 1999)

The Examiner rejected claims 1, 2, 4-12, 14-22, and 24-30 under 35 U.S.C. § 102(e) as anticipated by Rajsuman (Ans. 2-5).

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Briefs and the Answer[4] for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

THE ANTICIPATION REJECTION

Regarding the independent claims, the Examiner finds that Rajsuman discloses all of the claimed subject matter including a main system CPU 62 corresponding to the recited test scenario manager[5] and plural interconnected verification units that correspond to the recited signal interface controllers. According to the Examiner, the test scenario manager includes a shared data memory into which the signal interface controllers may store data since data can flow between the verification units and the CPU. (Ans. 3-8.)

[4] Throughout this opinion, we refer to (1) the Appeal Brief filed September 28, 2007; (2) the Examiner's Answer mailed November 26, 2007; and (3) the Reply Brief filed January 25, 2008.

[5] Although the Examiner never specifically maps the main system CPU 62 to the recited test scenario manager in the Answer, we nonetheless infer that the Examiner intended this correspondence in light of the Examiner's analysis which indicates that the Main CPU 62 includes the shared data memory—a feature that is part of the test scenario manager as claimed. *See, e.g.*, Ans. 8 ("Since the *Main CPU* carries out synchronization, response evaluation of cores, timing evaluations, and overall SoC [system-on-a-chip] evaluation, etc. *the Main CPU possesses the shared data memory* to allow for complete evaluation of the SoC.") (Emphasis added, original emphasis omitted). *Accord* Reply Br. 2 (noting that the Examiner maps the system CPU 62 to the recited test scenario manager).

Appellant argues that Rajsuman's main system CPU 62 (i.e., the test scenario manager) does not include a shared data memory that can be read by other signal interface controllers as claimed. (App. Br. 7-12; Reply Br. 2-3.) Although Appellant acknowledges that the verification units are interconnected together via a bus, Appellant emphasizes that the verification units do not communicate with each other via a shared memory in the CPU 62. (App. Br. 10; Reply Br. 3.)

Appellant adds that Rajsuman does not store data independent of advancement of simulated time as claimed. Appellant notes Rajsuman's synchronization differs from the claimed time generator which specifies events corresponding to simulated time—not real time. As such, this feature allows information to be passed while the time for the simulation itself is stopped. (App. Br. 12-14; Reply Br. 3-6.)

The issue before us, then, is as follows:

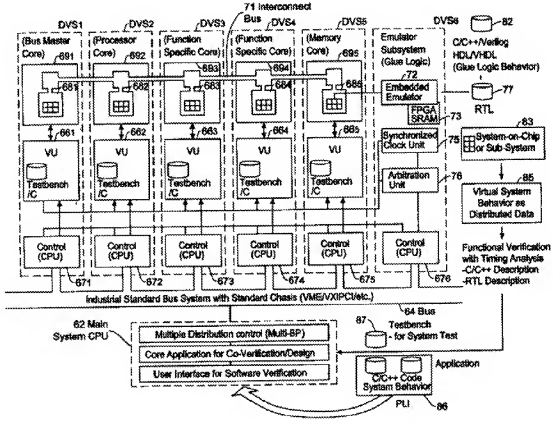
ISSUE

Under § 102, has Appellant shown that the Examiner erred in finding that Rajsuman discloses a test scenario manager that includes a shared data memory into which a signal interface controller may store data independently of advancement of simulated time, the data being readable from the shared data memory by another signal interface controller as recited in claim 1?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence:

1. Rajsuman discloses a system for validating system-on-a-chip (SoC) designs. In one implementation, a design validation station 50 comprises a main system CPU 62 connected to plural verification units (VUs) 66_1-66_5 via bus 64. The VUs are allocated to silicon ICs 68_1-68_N associated with respective "cores" A-N of the SoC. (Rajsuman, col. 7, ll. 15-59; Figs. 4B, 5.) Figure 5 illustrates a design validation station with plural VUs and is reproduced below:



Reproduction of Rajsuman's Figure 5 Showing Design Validation Station and Plural VUs

2. Each VU contains a control CPU 67 that controls data flow, application of simulation data to the silicon ICs, response comparison, scheduling, and status monitoring of individual cores and the SoC. (Rajsuman, col. 7, ll. 60-65; Fig. 5.)

3. The control CPUs 67_1-67_6 are connected with one another and connected to the main system CPU via the bus system 64. A synchronization unit 75 and an arbitration unit 76 promote data transfer to and from the main system CPU 62 and the control CPUs 67_1-67_6. (Rajsuman, col. 7, l. 65 – col. 8, l. 5; Fig. 5.)

4. Each VU is configured as an event tester and includes a control CPU 67, a failure memory 87, and an event memory 90. The failure memory stores test results (e.g., failure information of the silicon IC 68) with the address information provided by address sequencer 88. The stored failure information is used in the failure analysis stage of the cores and SoC. (Rajsuman, col. 9, l. 33 – col. 10, l. 12; Fig. 6.)

5. To verify the SoC as a system, the main system CPU 62 performs a "Fork" operation on an application task by breaking it down into multiple sub-tasks and assigning them to different VUs mapped to individual cores. These sub-tasks are distributed to individual VUs via system bus 64. The control CPU 67, arbitration unit 76, and synchronization clock unit 75 enable communication and error-free data transfer from the main system CPU 62 to the VUs' control CPUs 67. (Rajsuman, col. 12, ll. 15-35; Fig. 9.)

6. Based on the sub-task assignments, the control CPUs then apply event-based vectors to the individual cores and collect responses that are passed to the main system CPU 62. The main system CPU performs a "Join" operation to merge various responses and form a SoC-level response.

This response is compared with the simulation response to determine if the SoC performed correctly. (Rajsuman, col. 12, ll. 36-45; Fig. 9.)

7. Figure 11 shows another example of a design validation station where the main system computer 62 controls multiple VUs. Unlike other embodiments, the VUs in this embodiment do not include a control CPU. As such, all tasks (synchronization, response evaluation, overall SoC evaluation, etc.) are performed by the main system computer 62. (Rajsuman, col. 13, ll. 7-15; Fig. 11.)

PRINCIPLES OF LAW

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Appl. Dig. Data Sys., Inc.*, 730 F.2d 1440, 1444 (Fed. Cir. 1984); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983).

ANALYSIS

Based on the record before us, we find error in the Examiner's anticipation rejection of independent claim 1 which calls for, in pertinent part, a test scenario manager that includes a shared data memory into which a signal interface controller may store data that is readable by another signal interface controller.

First, we agree with the Examiner (Ans. 8) that Rajsuman's main CPU (i.e., the test scenario manager) performs synchronization, core response and

timing evaluations, and overall SoC evaluations. *See* FF 5-7. This functionality, however, hardly means that the test scenario manager would have a *shared data memory* that is readable by multiple signal interface controllers (i.e., VUs), let alone that another VU could store data in this shared memory independent of simulated time as claimed.

Rather, data is sent from the main CPU to particular VUs (e.g., in the form of sub-tasks) via bus system 64. (FF 3, 5, 7.) Based on these sub-task assignments, the VUs' control CPUs then apply event-based vectors to the individual cores and collect responses that are passed to the main system CPU 62. (FF 6.) The main system CPU then merges various responses from the VUs, and ultimately forms a SoC-level response that is compared with the simulation response to determine if the SoC performed correctly. (*Id.*)

While this merging and evaluation operation would certainly use a memory in the main system CPU 62 that would store data retrieved from multiple VUs for analysis, the Examiner has not shown—nor can we find—anything in Rajsuman that would indicate that this memory is a shared data memory *readable by different VUs*. This is a critical point: claim 1 does not merely recite a data memory in the test scenario manager, but rather a *shared* data memory that stores data from a signal interface controller that is *readable* by *another* signal interface controller. At best, Rajsuman's VUs merely send their individual test data to the main system CPU for evaluation, but the VUs do not *read* this data from the main CPU, let alone read *other* VUs' data. *See* FF 3-7.

To be sure, each VU has its own control CPU that is connected to other VUs' control CPUs and the main CPU via bus system 64 for data

transfer therebetween. (FF 3.) Not only does each VU's control CPU control, among other things, data flow and response comparison (FF 2), but each VU also has its own memory that stores test results (i.e., failure information) used for failure analysis. (FF 4.)

Nevertheless, despite the VUs' interconnection via a bus (FF 3) and their "response comparison" capabilities (FF 2)—a feature that suggests some sort of ability to compare responses from either the same or different VUs—there is nothing in Rajsuman that actually states that the test scenario manager (i.e., the main system CPU) would have a shared data memory readable by other signal interface controllers (i.e., VUs) as claimed. The Examiner's contentions to the contrary (Ans. 8) are unavailing.

Additionally, to the extent that the Examiner's position is predicated on the notion that an individual VU's control CPU (*see* FF 2-4) somehow constitutes a "test scenario manager,"[6] we find this alternative interpretation problematic. Even if we assume, without deciding, that a particular VU can control its individual test regimen for its particular silicon IC core via its internal CPU (*see id.*), the Examiner has not shown how a particular VU can function as a "test scenario manager" with its requisite recited control functions with respect to the other signal interface controllers (which are also said to correspond to the VUs (Ans. 3)). We therefore find this alternative interpretation untenable.

We also agree with Appellant (App. Br. 12-14; Reply Br. 3-6) that Rajsuman does not store data independent of advancement of simulated time

[6] *See, e.g.*, Ans. 7 ("Since the VU's [sic] are connected to each other as well as the CPU *they therefore possess a shared memory* in which tasks such as synchronization and overall evaluation must be carried out by utilizing multiple VUs.").

as claimed. Even if we assume, without deciding, that Rajsuman executes different parts of the SoC at different times as the Examiner contends (Ans. 11), this hardly means that data is stored independently of *simulated* time for the hardware simulator as claimed. As Appellant indicates (Reply Br. 4-5), Rajsuman's synchronizing clock 75 synchronizes the VUs—not the silicon ICs. *See* FF 3 and 5. There is simply nothing in Rajsuman to suggest that data is stored independently of simulated time for the hardware simulator as claimed.

For the foregoing reasons, Appellant has persuaded us of error in the Examiner's rejection of independent claim 1, and independent claims 11 and 21 which recite commensurate limitations. Therefore, we will not sustain the Examiner's rejection of those claims, and dependent claims 2, 4-10, 12, 14-20, 22, and 24-30 for similar reasons.

CONCLUSION

Appellant has shown that the Examiner erred in rejecting claims 1, 2, 4-12, 14-22, and 24-30 under § 102.

ORDER

The Examiner's decision rejecting claims 1, 2, 4-12, 14-22, and 24-30 is reversed.

REVERSED

pgc

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